Flexibility - a long term solution to DCI compliance

Keith Morris, Marketing and Sales Manager of intoPIX, but perhaps better known to BKSTS Members from his previous work on Digital Cinema with Barco, explains how the move to the all-important 'DCI Compliance' is going to affect all of us in the digital cinema business.

Scratch the polished surface of Digital Cinema these days and behind the stunning presentations, declarations of ever increasing numbers of Digital screen installations and raft of new product introductions that is now ShoWest and you quickly discover another reality - 'DCI' and the language of 'Interoperability' and 'Compliance'.

Since long before its publication in July 2005 the Digital Cinema Initiative (DCI) recommendations document (1) - the tablet of stone that now defines 'Digital Cinema' - has been exhaustively combed by equipment manufacturers for its deeper meaning, and potential cost implications.

….. Just how will server and projector manufacturers interpret FIPS security certification (2)
….. meet the JPEG2000 compression standard (3), and
….. what indeed will constitute acceptable Watermarking?

In this context is the so called 'Media Block' a realist proposition and if so, by when? How is it defined, and is it better located in the Digital Projector or the Server?

These may be mature considerations but, if the feedback from ShoWest'06 is any measure, these issues now have to be dealt with urgently to achieve the Hollywood's desire to implement the JPEG 2000 compression standard this year, ahead of the deployment of significant quantities of digital screens in 2007, and to fully enable the (only slightly) longer term promise of 4K, 3D and, who knows, even 4K 3D display!

How *will* manufactures meet the multiple objectives of
- ensuring that they are quickly and fully DCI compliant, while
- attaining true Interoperability, while
- ensuring that they are sufficiently prepared for the variable cocktail of D & E cinema, digital broadcast and advertising display that is the future?

All of which raises intriguing questions regarding today's technology …
Can it deliver the necessary processing power to meet even more demanding future applications …or the flexibility to provide an affordable, and manageable, migration path?

And questions of functionality. In the context of 153 pages of DCI specifications encompassing such matters as DCDM (Digital Systems Digital Mastering), Security, Packaging, Compression, Digital Certificate, Extra-Theater Messages (ETM), and Key Delivery Messages (KDM) requirements, what are the priorities. Just where do we start?

Today's technologies

Behind the discussion about whether a Texas Instruments (2K resolution) or Sony (4K) 'Digital Eye' is most desirable, there is another - about the 'Digital Brain', its form, function, and for some, even the location of the core intelligence that drives the D-Eye.

Three processing technologies exist today to provide this processing intelligence - ASIC, DSP and FPGA.

Of these, ASIC is the most well established and is the processing intelligence incorporated in the majority of today's Digital Cinema servers. [Application Specific Integrated Circuits, i.e. ICs designed for a particular application, as opposed to ICs such as those for RAM in a PC, are built by connecting circuit 'building blocks' together. The blocks already exist in a library, so it is easier to produce a new ASIC than to design a new chip from scratch.]

However an ASIC is essentially a dedicated device with a fixed functionality and insufficient inherent processing power to meet the needs of an increasingly complex Digital Cinema requirement. Even today a minimum of three ASIC chips are needed to process at 2K resolution and, depending on the architecture, fifteen or more, *plus* an FPGA controller [Field Programmable Gate Array], will be required for 4K use.

Secondly the use of DSP (Digital Signal Processor) architecture provides an interesting possibility considering its software based reprogrammability and the resulting greater flexibility. It too though has its limits, specifically in its ability to efficiently meet the precise, real time, requirements of entropy decoding – the most critical of all of the many image compression blocks. [Entropy encoders compress data by assigning codes to symbols so as to match code lengths with the probabilities of the symbols - the most common symbols use the shortest codes.]

The third technology uses FPGA, a field-programmable gate array; a semiconductor containing both remotely programmable logic components and standard interfaces.

Power and Flexibility

At a first glance FPGA appears a strong option. It has the processing power needed for future display applications, its re-programmability containing the promise of cost effective new product development, and its ability to be reprogrammed on-site easing the (potentially considerable) burden of bug fixing first generation display networks.

Additionally FPGA also incorporates both a DSP block for the benefits of its arithmetic computation and benefits from the software flexibility of an on-board CPU. It is then an ideal host for a full a Media Block, and further more, one that can be equipped with reprogrammable Ethernet, SATA and HD-SDI output links.

Even more compelling still however is the FPGA's high level process integration and its compact physical size, both of which provide significant processing and physical security advantages.

What Comes First?

DCI compliance is indeed a daunting prospect for most equipment providers.

Just how and when will manufacturers achieve full DCI compliance when, for example, the FIPS [Federal Information processing Standards] and Watermarking security requirements are still being debated,

and DCI compliance procedures have not yet been defined, is still an open question.

While the industry holds its breath on these and many other detailed issues however, the one certain, immediate and realizable reality is the DCI adoption of the JPEG 2000 compression format in place of the MPEG system currently incorporated into most Digital Cinema servers. Since its publication in Y2K the Wavelet based JPEG 2000 compression algorithm has been noted for its extreme flexibility – but regarding Digital Cinema applications particularly – it provides the benefits of frame-by-frame multi-level access (e.g. for single frame editing), and also allows users to address specific 'regions of interest' and define up to lossless output quality. And so, assisted by Hollywood Studio demands that providers move quickly, the race for JPEG 2000 compliance is on!

Meeting the challenge

'Cue' Belgium to take its place on the leading edge of the Digital Cinema discussion again!

In another of a succession of the country's Digital Cinema innovations the management of one of Belgium's leading technology universities, the Université catholique de Louvain (UCL), recognized the technology challenge in 2001 and made the visionary decision to investigate the suitability of JPEG 2000 compression for Digital Cinema, in the context of its internationally recognized expertise in the relatively new field of FPGA technology.

Pre-empting the DCI decision on compression standards by a full four years, UCL consolidated the JPEG development programs of three of its laboratories, and set about a mission to develop secure handling tools for high quality, high throughput and high value data streams. And now, in another timely decision, UCL is launching the resulting IPs [Intellectual Properties] through intoPIX, a Belgian technology company, to market a range of FPGA based solutions that meet the DCI specifications but, wisely it transpires, are also capable of much more.

Building on over 15 man-years management experience UCL and intoPIX associates have in fact been making significant contributions to the JPEG 2000 and Digital Cinema standardization committees since 2001 – most recently through UCL's involvement as a repository for the JPEG committee's Digital Cinema Interoperability Test Plan.

Currently UCL and intoPIX associates are also project managing the EU 'EDCine' program; a project commencing in June involving a consortium of 16 European organizations (including the Fraunhofer Institute appointed by DCI to define its Compliance Test Procedures) who will look even further into the Digital Cinema crystal ball.

By thinking beyond DCI and pushing the limits of SMPTE specifications (4) the EDCine project aims to still further enhance the Digital Cinema experience by investigating quality optimization issues, robustness to transmission errors, content security tools, stereoscopic imaging, interactive access, forensic marking and metadata for indexing and retrieval.

The intoPIX solution:

It's against this background then that intoPIX has defined three strategic objectives in developing its own, highly integrated, and flexible media-block solution:

- First, and most important, that it should meet &, wherever possible, exceed DCI compliancy requirements.
- Secondly that it should be expert in FIPS Levels 3 and 4 certification requirements.
- And third that it provide a flexible solution; one based on a family of IP's that are both inherently flexible and also be 'mixed and matched' to fit the differing requirements of individual users.

And it is in recognition of the importance of this final key objective in particular (to provide a flexible and therefore future-proof solution) that has ultimately decided the company to develop its IPs on the FPGA platform.

IPX-JP2K decoder module

Currently intoPIX is proposing two key FPGA based IP cores, one for the JPEG 2000 decoder (the IPX-JP2K) and an AES encryption/decryption (the IPX-AES) module.

The first of these, the IPX-JP2K JPEG 2000 decoder module, is based on the Xilinx Virtex-4 FPGA and specifically intended to meet the needs of a Digital Cinema playback system. In achieving the objective of providing a flexible family of IP's, the IPX-JP2K compression core is entirely compatible with other core IPs such as the company's own AES security core.

Just as important for the Digital Cinema system operator however is the IP's efficient combination of on-chip hardware and software operations and optimal co-design repartition of the decoding blocks (illustrated below) that provide the IPX-JP2K a unique post-deployment renewability for field upgrade and update.

The IPX-JP2K core

JPEG 2000 parser

The JPEG 2000 parser analyses the main and tile-part headers of the JPEG 2000 codestream, checks the syntax, reports images properties and sends the compressed bit-stream to the entropy decoder. The parser is developed in software running on a microblaze.

Entropy decoder

The reconstruction of each wavelet subband divided into several code-blocks is achieved by two blocks: the *Context Modeller* and the *Arithmetic Decoder.* The Context Modeller successively decodes each bit-plane of the code-block by sending information describing the neighborhood of each bit to the Arithmetic Decoder. With this information, the Arithmetic Decoder decodes each bit from the bit-stream.

Inverse Quantizer

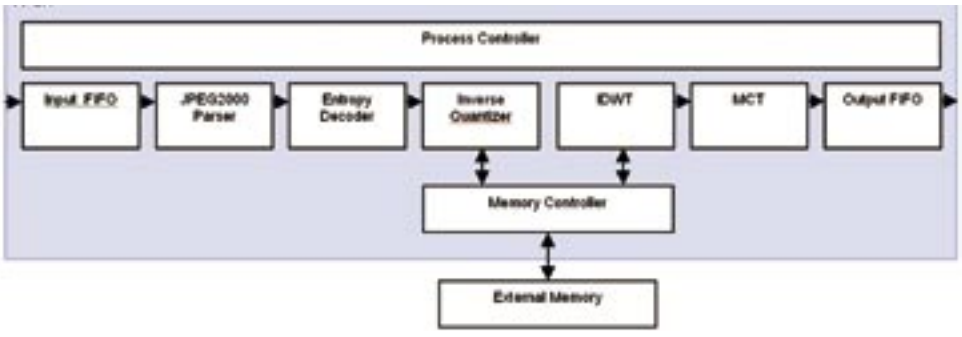
The coefficients of the wavelet subbands are inverse quantized. The quantization steps are defined in the main header of the JPEG 2000 file and can be different for each subband. The inverse quantizer uses up to date Xilinx Virtex-4 features (such as DSP blocks).

External memory

A double frame memory buffer is used at the Inverse Quantizer output and enables an efficient IDWT processing. This buffer, containing two DDR-SDRAM external memories, always keeps at least one valid frame that could be repeated when convenient. The required DDR-SDRAM type is a 512 Mbit memory (32 Meg x 16; 133 MHz for 2K and 48 fps). The frame buffer is able to store 4 frames at maximum.

Inverse Discrete Wavelet Transform (IDWT)

A bidimensional wavelet recomposition of the subbands is achieved. Two filter banks, with a 18-bit fixed point precision, may



be used: either the Le Gall (5/3) filter bank prescribed for lossless encoding or either the more complex Daubechies (9/7) filter bank for lossy encoding. In DC application only a 9/7 filter is required.

Multiple component transformation (MCT)

In order to improve the JPEG 2000 compression efficiency , multiple component transformations can be used. The reversible transform (RCT) is used with the 5/3 filter, and the irreversible transform (ICT) with the 9/7 filter. Both transformations are implemented with a 18-bit fixed point precision.

Error Handling

The decoder is designed to detect errors in the input data. This detection is achieved at two levels:

- JPEG 2000 header

Codestream characteristics such as image size and bits per components are checked. The coherence of the J2K headers with the specifications given by the decoder controller is analyzed.

- JPEG 2000 packet headers and compressed bit-stream

Packet headers are analyzed to verify the coherence of tag trees, number of bit-planes and code-block compressed bitstream length.

When an error is detected, specific error codes are sent to the device managing the decoder. In the case of a corrupted frame codestream, the decoder will decode the next frame and repeat it until a correct frame is encountered. If no frame can be decoded during the elapsed time determined by the frame rate, the previous correctly decoded frame is sent to the output to avoid any unpleasant display artifacts.

Process Control

Taking advantage of the JPEG 2000 intra-frame coding, the decoder controller can manage the stream at the frame accuracy. When there is no data to decode at its input, the decoder can loop on the latest decoded frame, output a black frame or stop processing. And by controlling the input stream and the output options, the decoder controller manages *Pause, step by step, slow-motion, fast forward* and *rewind*, and random *access*.

Interfaces

The input receives data by 32-bit bursts of in Little-Endian representation. A burst of two pixels (RGB, XYZ or YUV) is output. The output clock depends on the sequence frame rate and picture size.

DCI plus

In attempting to achieve the first of its key objectives intoPIX has, from the beginning, set itself the challenge of beating the current DCI requirements wherever possible and, in this respect also too, the IPX-JP2K IP appears to succeed.

As demonstrated in the following chart comparing today's DCI requirements with the performance intoPIX has anticipated, a considerable technology evolution in the key areas of input and output bit rates, frame rates and colour depth; while also allowing for a considerable variety of screen sizes up to 2048 x 1080, and RGB, YUV or XYZ output types.

The major advantage of IPX-JP2K is indeed its ability to manage with higher input and output bit-rates.

While current DCI input bit rate is 250 Mbps for all compressed content (2K @ 24/48 and 4K @ 24 frames per second) the IPX-JP2K provides output rates of up to 500 Mbps making the IP ready well in advance of the possibility of higher frame rate 4K requirements. This future IP will be called the IPX-JP4K and be available soon in Virtex-4 FX60 technology.

Again, anticipating 3D display requirements, the JP2K operates at up to 96 fps

Also, in another example of its forward thinking, the intoPIX decoder exceeds the DCI 12 bits color depth requirement to deliver an ample14 bits per component.

And last but not least, recognizing the special needs of several other potential IP user groups the intoPIX decoder provides the opportunity to manage multiple quality layers allowing archivists for instance to create a unique 2K file, 48 fps, 500 Mbps, or to for instance allow one decoder to decompress the 250 Mbps layer only, while a second decoder decompresses all other layers representing, in total, 500 Mbps.

The end game – Compliance

It seems only yesterday that the Cinema industry was vociferously concerned about being driven (unnecessarily) by technologists. Today however there's no doubt that market forces are back in the driving seat.

To quote John Fithian, President of NATO in his keynote address at the Digital Cinema summit at NAB this year "2006 is the big year for Digital Cinema; the DCI standards, quality and business models are there. Digital Cinema is on the bell curve … 2007 will be huge"

It's no surprise then that, with digital installations forecast to grow from 1000 to over 2000 by the end of the year, there is pressure from Hollywood for immediate action to meet as many the DCI requirements as quickly as possible.

The work of developers has taken on a new sense of urgency and, obliged to act ahead of the publication of Compliance procedures, Digital Cinema equipment providers are, once again, required to apply the Wisdom of Solomon.

Specifications	DCI requirements	IPX-JP2K features
Image Coding Format	JPEG 2000 : ISO/IEC 15444-1	JPEG 2000 : ISO/IEC 15444-1
Wavelet Transform Filter	9/7 filter: 16-bit fixed point precision	5/3 and 9/7 filter: 18-bit fixed point precision
Tiles	Single tiles	Single or multiple tiles
Quality Layer	Single quality layer	Single quality layer (Multiple quality layer: optional)
Resolutions	Up to 6 resolutions	Up to 7 resolutions
Code Block size	32x32 pixels	32x32 pixels
Code Block coding style	Standard JPEG 2000 options	Standard JPEG 2000 options (Parallel Mode optional)
Input data-rate	Up to 250 Mbit/s	Up to 500 Mbit/s
Image size	Up to 2048 x 1080 pixels (for 2K content)	Up to 2048 x 1080 pixels (JP2K)
Frame-rate	Up to 48 FPS	Up to 96 FPS
Output throughput	Up to 3,8 Gbit/s	Up to 7,6 Gbit/s
Component transform	ICT 16-bit fixed point precision	RCT and ICT 18-bit fixed point precision
Color output format	XYZ	RGB, XYZ and YUV
Color Depth	Up to 12 bits per component	Up to 14 bits per component
Recommended FPGA	No recommended solution	Virtex-4 SX35

However the industry-wide scrutiny of the DCI protracted specification process does provide some clues. Informed anticipation and more than a shake of inspiration has ensured an elegant solution to at least the 'known quantity' of JPEG2000 compression.

And if this can be made available in a 'host' processor that also eases the development path for manufacturers, assists Hollywood's security concerns, provides logistical benefits to Network operators *and* supports the 4k and 3D future of Exhibitors then surely so-much-the-better.

References:
[1] Digital Cinema Initiatives, LLC, "Digital Cinema System Specification V1.0", July 20, 2005.
[2] Federal Information Processing Standards, "FIPS 140-2 Security Requirements for Cryptographic Modules", May 2001.
[3] ISO/IEC 15444-1: Information Technology-JPEG 2000 image coding system-Part 1: Core coding system, 2000.
[4] Society of Motion Picture and Television Engineers, DC28 Digital Cinema Technology Committee. Authors: Gael Rouvroy CTO / Keith Morris, Marketing Manager intoPIX s.a.

For further information on the IPX-JP2K and IPX-AES IP modules and intoPIX scientific publications visit: www.intopix.com

About intoPIX

intoPIX is an independent image technology company with mission to develop and market secure handling tools for high quality, high throughput and intrinsically high value data streams.

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EXPERTISE
Working closely with the Université Catholique de Louvain in Belgium intoPIX benefits from the knowledge and facilities of the University's advanced Compression, Cryptographic and Micro-electronics laboratories. Bringing together world-class expertise, intoPIX works on the leading edge of JPEG2000 image management and its implementation in the latest generation FPGA chips.

MARKETS
Building on over 15 man-years management experience, intoPIX associates have made significant contributions to the JPEG2000 and Digital Cinema standardization committees since 2001, and now also lead the way with cost effective solutions for Digital Acquisition, Post Production, Distribution and Archiving.

into**PIX** s.a.
place du Levant 3
B-1348 Louvain-la Neuve